WHAT IS CLAIMED IS:

1. A data processing system comprising: a first semiconductor integrated circuit; a second semiconductor integrated circuit; a transmission line that connects a first external output buffer of the first semiconductor integrated circuit to the second semiconductor integrated circuit, and connects a second external output buffer of the second semiconductor integrated circuit to the first semiconductor integrated circuit; and an external power supply circuit that generates an operational supply voltage to the first and the second external output buffers,

wherein the first semiconductor integrated circuit instructs the external power supply circuit to be able to modify a level of the operational supply voltage, and includes a first operation mode capable of selectively controlling an output transistor size of the first external output buffer according to the operational supply voltage supplied according to the instruction, and

wherein the second semiconductor integrated circuit includes a second operation mode capable of selectively controlling the output transistor size of the second external output buffer according to the operational supply voltage supplied from the external power supply circuit.

2 A data processing system comprising: a first semiconductor integrated circuit; a second semiconductor integrated circuit; and a transmission line that connects a first external output buffer of the first semiconductor integrated circuit to the second semiconductor integrated circuit, and connects a second external output buffer of the second semiconductor integrated circuit to the first semiconductor integrated circuit,

wherein the first semiconductor integrated circuit includes an internal power supply circuit that generates an operational supply voltage to the first and the second external output buffers, instructs the internal power supply circuit to be able to modify a level of the operational supply voltage, and includes a first operation mode capable of selectively controlling an output transistor size of the first external output buffer according to the operational supply voltage generated according to the instruction, and

wherein the second semiconductor integrated circuit includes a second operation mode capable of selectively controlling the output transistor size of the

second external output buffer according to the operational supply voltage supplied from the internal power supply circuit of the first semiconductor integrated circuit.

3. A data processing system according to Claim 2

wherein in the first operation mode, the first semiconductor integrated circuit selectively controls the output transistor size according to the operational supply voltage, in a direction of making an impedance matching of the transmission line and the first external output buffer, and

wherein in the second operation mode, the second semiconductor integrated circuit selectively controls the output transistor size according to the operational supply voltage, in a direction of making the impedance matching of the transmission line and the first external output buffer.

4. A data processing system according to Claim 3,

wherein in the first operation mode, when it is impossible to select the output transistor size for making the impedance matching, the first semiconductor integrated circuit modifies to designate a level of the operational supply voltage, and redoes the selective control of the output transistor size, and

wherein in the second operation mode, when it is impossible to select the output transistor size for making the impedance matching, the second semiconductor integrated circuit instructs the first semiconductor integrated circuit to modify the level of the operational supply voltage, and redoes the selective control of the output transistor size according to a modified operational supply voltage.

5. A data processing system according to Claim 3,

wherein in the first mode, the first semiconductor integrated circuit outputs first information to designate a level of the operational supply voltage, selectively controls the output transistor size according to the operational supply voltage answered in response to the first information, requests to modify the operational supply voltage by means of the first information to redo selecting the output transistor size when it is impossible to select the output transistor size for making the impedance matching, outputs second information to the outside, waits for third information

answered from the second semiconductor integrated circuit to the second information, requests to modify the operational supply voltage by means of the first information to redo selecting the output transistor size, waits for fourth information answered from the second semiconductor integrated circuit to the second information, and completes the selective control of the output transistor size,

wherein in the second mode, the second semiconductor integrated circuit inputs the second information from the first semiconductor integrated circuit, starts the selective control of the output transistor size according to the operational supply voltage by responding to the second information, outputs the third information to the first semiconductor integrated circuit when it is impossible to select the output transistor size for making the impedance matching, and outputs the fourth information to the first semiconductor integrated circuit when it is possible to select the output transistor size for making the impedance matching.

6. A data processing system according to Claim 1, wherein the first semiconductor integrated circuit executes, in the first operation mode, a designation of the operational supply voltage from a lower level, and execute a selection of the output transistor size from a larger size.

7. A data processing system according to Claim 1,

wherein the first and the second semiconductor integrated circuits are individually capable of detecting error rates of data transmitted thereto,

wherein in the first operation mode, the first semiconductor integrated circuit is capable of a selection-modification control of the output transistor size while increasing the operational supply voltage, until the sum of the error rates detected individually by the first and the second semiconductor integrated circuits becomes lower than a specified value, and

wherein in the second operation mode, the second semiconductor integrated circuit is capable of responding to the selection-modification control by the first semiconductor integrated circuit, and capable of the selection-modification control of the output transistor size to the operational supply voltage modified by the instruction of the first semiconductor integrated circuit.

8. A data processing system according to Claim 1,

wherein the first semiconductor integrated circuit is specified as being in the first operation mode, starting with responding to a system reset until reaching an impedance matching between the transmission line and the first external output buffer, in which, in response to an arrival of a specific interval, an impedance mismatching between the transmission line and the first external output buffer is compensated by a specific amount to the matching direction, and

wherein the second semiconductor integrated circuit is specified as being in the second operation mode, starting with responding to the system reset until reaching an impedance matching between the transmission line and the second external output buffer, in which, in response to the arrival of the specific interval, an impedance mismatching between the transmission line and the second external output buffer is compensated by the specific amount to the matching direction.

9. A data processing system according to Claim 8, wherein the first semiconductor integrated circuit detects the arrival of the specific interval.

10. A data processing system according to Claim 1, comprising a plurality of the second semiconductor integrated circuits, wherein the plural second semiconductor integrated circuits are connected to the first semiconductor integrated circuit by individual transmission lines, and the operational supply voltage is individualized to each of the transmission lines.

11. A data processing system according to Claim 2 wherein the first semiconductor integrated circuit executes, in the first operation mode, a designation of the operational supply voltage from a lower level, and execute a selection of the output transistor size from a larger size.

12 A data processing system according to Claim 2,

wherein the first and the second semiconductor integrated circuits are individually capable of detecting error rates of data transmitted thereto,

wherein in the first operation mode, the first semiconductor integrated circuit is capable of a selection-modification control of the output transistor size while increasing the operational supply voltage, until the sum of the error rates detected individually by the first and the second semiconductor integrated circuits becomes lower than a specified value, and

wherein in the second operation mode, the second semiconductor integrated circuit is capable of responding to the selection-modification control by the first semiconductor integrated circuit, and capable of the selection-modification control of the output transistor size to the operational supply voltage modified by the instruction of the first semiconductor integrated circuit.

13. A data processing system according to Claim 2,

wherein the first semiconductor integrated circuit is specified as being in the first operation mode, starting with responding to a system reset until reaching an impedance matching between the transmission line and the first external output buffer, in which, in response to an arrival of a specific interval, an impedance mismatching between the transmission line and the first external output buffer is compensated by a specific amount to the matching direction, and

wherein the second semiconductor integrated circuit is specified as being in the second operation mode, starting with responding to the system reset until reaching an impedance matching between the transmission line and the second external output buffer, in which, in response to the arrival of the specific interval, an impedance mismatching between the transmission line and the second external output buffer is compensated by the specific amount to the matching direction.

14. A data processing system according to Claim 13, wherein the first semiconductor integrated circuit detects the arrival of the specific interval.

15. A data processing system according to Claim 2, comprising a plurality of the second semiconductor integrated circuits, wherein the plural second semiconductor integrated circuits are connected to the first semiconductor integrated circuit by individual

transmission lines, and the operational supply voltage is individualized to each of the transmission lines.